NATURAL ENVIRONMENT RESEARCH COUNCIL

EPSRC

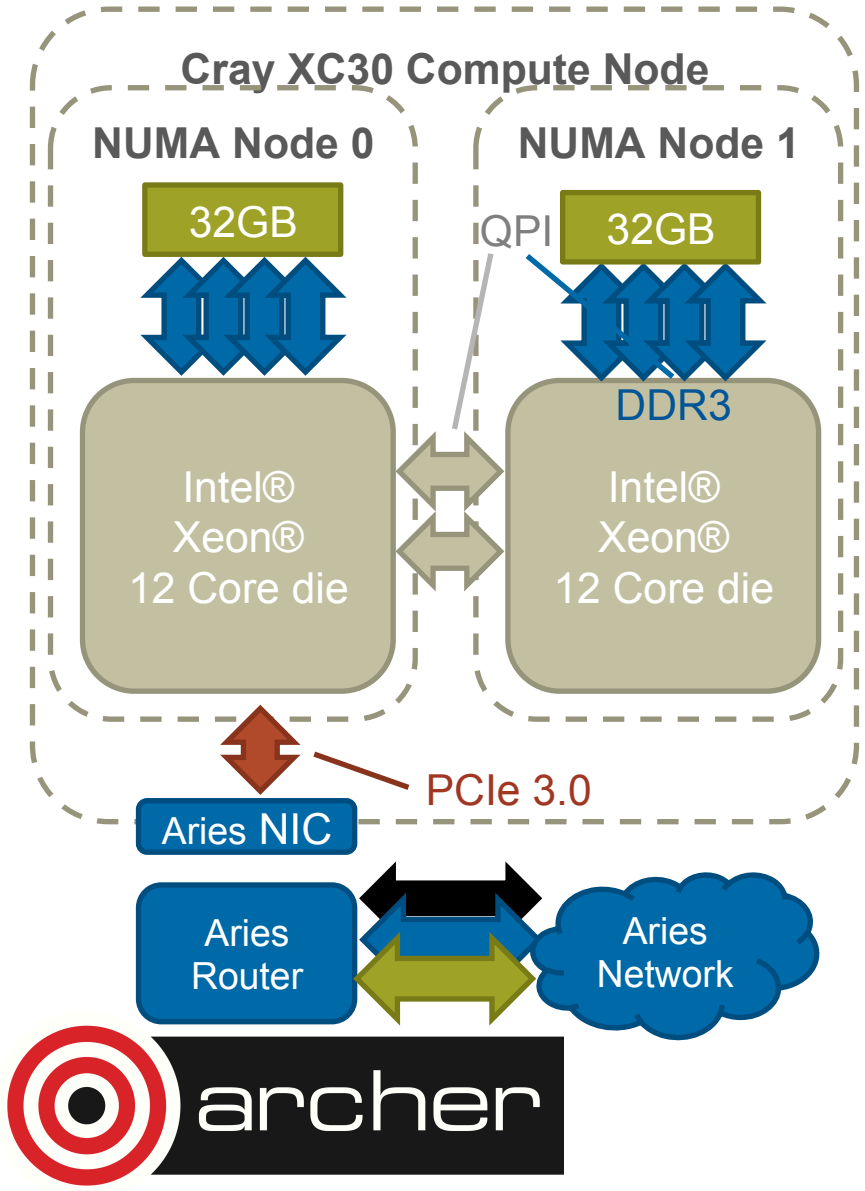
ARCHER Single Node Optimisation

ARCHER Node Architecture

Slides contributed by Cray and EPCC

epcc

Cray XC30 Intel® Xeon® Compute Node



The XC30 Compute node features:

- 2 x Intel® Xeon® Sockets/die
  - 12 core Ivy Bridge
  - QPI interconnect
  - Forms 2 NUMA nodes
- 8 x 1833MHz DDR3
  - 8 GB per Channel
  - 64/128 GB total
- 1 x Aries NIC
  - Connects to shared Aries router and wider network
  - PCI-e 3.0

epcc | THE UNIVERSITY OF EDINBURGH

Intel Ivy Bridge Processor

- Proper name: Xeon E5-2697v2
- No. of cores = 12
- Clock rate = 2.7 GHz
- 1 FP adder, 1 FP multiply (no FMA)
- 256-bit wide AVX vector instructions
  - 4 double precision floating point ops
- Peak 8 flops per clock = 21.6 Gflop/s per core = 259 Gflop/s per socket = 518 Gflop/s per node
- Up to two hardware threads (hyperthreads) per core

Memory hierarchy

- Each core has
  - Level 1 cache: 32 KB, 8-way set associative, 64 byte lines
  - Level 2 cache: 256 KB, 8-way set associative, 64 byte lines
- All 12 cores share one Level 3 cache
  - 30 MB, 16-way set associative, 64 byte lines
  - 2.5MB per core
- 64 GB main memory per node (128 GB on high memory nodes) in 2 NUMA regions (1 per socket)
- Bandwidths per core L1/L2/L3/Mem = 100/40/20/4 GB/s
- Memory latency = ~80ns (~210 clock cycles)